Serial No.: 09/841,077 Docket No.: 024016-00008

REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By the foregoing amendment, claims 1 and 10-12 have been amended. Claims 8 and 17 have been previously canceled. Thus, claims 1-7, 9-16, 18 and 19 are currently pending in the application and subject to examination.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this

Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims; and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

In the Office Action mailed May 30, 2006, the Examiner objected to claim 12 for informalities. Claim 12 has been amended responsive to the objection. If any additional amendment is necessary to overcome this objection, the Examiner is requested to contact the Applicant's undersigned representative.

The Examiner rejected claims 1-7, 9-16, 18 and 19 under 35 USC § 102(e), as being anticipated by Wilson et al. (U.S. Patent No. 6,118,603, hereinafter, "Wilson"). It is noted that claims 1 and 10-12 have been amended. To the extent that the rejection

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remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Each of independent claims 1 and 10, as amended, recites, in part:

a receiving unit for receiving the series of data including the predetermined mark for detecting synchronization and generating parallel data from the series of data; and

a plurality of detecting units being provided at each bit position of the parallel data, the detecting units being adapted to detect whether strings of bits of the parallel data corresponding to strings of bits of the series of data from each bit position of the parallel data as a starting point of the predetermined mark are the predetermined mark; and

wherein any one of the detecting units detects the starting point of the predetermined mark.

Thus, in the Applicants' invention as recited in independent claims 1 and 10, a receiving unit receives a series of data including a single predetermined mark and generates parallel data from the series of data. The predetermined mark, which detects synchronization of the series of data, is sequentially arranged, dividedly, bit by bit, at each bit position of the parallel data. Each of the plurality of detecting units is provided at each bit position of the parallel data. The detecting units are adapted to detect whether strings of bits of the parallel data, which correspond to strings of bits of the series of data, are the predetermined mark. The detecting units detect whether the strings of bits continuing from each bit position of the parallel data as a starting point of the predetermined mark, are the predetermined mark. Any one of the detecting units detects the starting point of the predetermined mark. Thus, in the claimed invention, detection of the predetermined mark is conducted by any one of the detecting units detecting the starting bit position of the predetermined mark in the parallel data.

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Independent claim 11, as amended, recites, in part:

receiving a series of data including a predetermined mark for detecting synchronization;

generating a parallel data from the series of data;

detecting the predetermined mark for detecting synchronization from any one of strings of bits of the parallel data continuing from each bit position of the parallel data to establish synchronization of the series of data; and

demodulating the series of data based on the predetermined mark for detecting synchronization detected from one of the bit strings.

Thus, in the Applicants' invention as recited in independent claim 11, as amended, a series of data including a predetermined mark for detecting synchronization of the series of data is received. Parallel data is generated from the series of data, and the predetermined mark is detected from any one of strings of bits of the parallel data continuing from each bit position of the parallel data to establish synchronization of the series of data. The series of data is demodulated based on the predetermined mark for detecting synchronization detected from one of the bit strings.

The Applicants respectfully submit that Wilson neither discloses nor suggests each and every feature recited in claims 1, 10 and 11, as amended.

The outstanding Office Action asserts that Wilson discloses a plurality of detecting units being provided at each bit position of the parallel data by the XNOR comparators 518 of Fig. 5. Further, the Office Action asserts that Wilson discloses "the detecting units being adapted to detect whether strings of bits continuing from each bit position as a starting point are the predetermined mark," by a mark match count signal 528 of Fig. 5, and that "any one of the detecting units detects the predetermined mark" by XNOR comparators 518 and at col. 8, lines 12-65. However, as disclosed by Wilson at col. 8, lines 12-65, each of the XNOR comparators 518 produces a mark bit

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comparison signal 524, and the mark bit comparison signals 524 <u>are summed to produce a mark match count signal 528</u>. The mark match count signal 528 is provided to a magnitude comparator 530 in <u>each</u> of majority vote circuits 515 and 516. The magnitude comparators 530 compare the mark match count signal 528 with a detection threshold 532 and output a signal indicating detection of a Servo Synchronizing Mark when 528 is greater than 532.

Thus, detection of a Servo Synchronizing Mark is conducted based on a combined output of all of the XNOR comparators 518. Wilson neither discloses nor even suggests that detection of a predetermined mark is performed by <u>one</u> of the XNOR comparators 518, as asserted by the outstanding Office Action.

Moreover, majority vote circuits 515 and 516 are distinct circuits which detect different marks, Mark_0 and Mark_1, respectively, by parallelizing serial data. In Wilson, if the majority vote circuits 515 and 516 fail to detect the respective synchronization marks, the synchronization can not be detected. Accordingly, the apparatus and method of Wilson cannot and do not detect a predetermined mark for synchronization by any one detecting unit, as recited in claims 1 and 10, nor is a predetermined mark detected from any one of strings of bits of the parallel data continuing from each bit position of the parallel data to establish synchronization of the series of data, as recited in claim 11.

For at least these reasons, the Applicants submit that independent claims 1, 10 and 11, as amended, are allowable over Wilson. As claims 1, 10 and 11 are allowable, the Applicants submit that claims 2-7, 9, 12-16, 18 and 19, each of which depends from

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one of allowable claims 1, 10 and 11, are likewise allowable for at least the reasons set

forth above with respect to claims 1, 10 and 11.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now

pending patentability distinguish the present invention from the cited references.

Accordingly, reconsideration and withdrawal of the outstanding rejections and an

issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this

application into better form, the Examiner is requested to contact the undersigned

representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby

petition for an appropriate extension of time. The fee for this extension may be charged

to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge

any fee deficiency or credit any overpayment associated with this communication to

Deposit Account No. 01-2300, referencing docket no. 024016-00008.

Respectfully submitted,

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Enclosures: Petition for extension of time

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